

As indicated above, claim 6 has been amended to delete the reference characters.

The Examiner has rejected claims 6-9 under 35 U.S.C. Section 102(b) as being anticipated by the Fazan, et al., patent.

For the reasons set forth below, this rejection is traversed as applied to amended claim 6.

Claim 6 has been amended to recite that the lower capacitor plate of the DRAM cell structure is formed by first forming a first layer of conductive material having a first thickness on the edges of the contact trench and then forming a second layer of conductive material having a second thickness that is less than the first thickness on the first layer.

Careful review of the Fazan, et al., disclosure shows that the reference neither teaches nor suggests this feature.

New claim 10, which depends from amended claim 6, further recites that the step of forming the conductive lower capacitor plate comprises depositing the first layer of polysilicon of a first thickness on the contact trench edges, then depositing a second layer of polysilicon having a lesser thickness than the first layer on the first layer, and patterning the two poly layers to define the lower capacitor plate.

New claim 11, which also depends from amended claim 6, has been added to recite that, after forming the layer of second dielectric material, a layer of thick conductive material is formed on the second dielectric material such that the contact trench formation step causes the contact trench to be formed in the conductive layer and in the second dielectric material.



Neither of the features recited by new claims 10 and 11 are either taught or suggested by the Fazan, et al., reference.

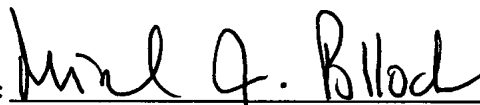
For the reasons set forth above, it is believed that all claims now present in the application are in compliance with the requirements of 35 U.S.C. Section 112 and patentably distinguish over the prior art. Therefore, it is requested that this application be passed to allowance.

Respectfully submitted,

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